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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/420,086	10/18/1999	WARREN M. FARNWORTH	98-0105.01	2322

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EXAMINER	
PAREKH, NITIN	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/420,086	Applicant(s) FARNWORTH ET AL.	
	Examiner Nitin Parekh	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-39 and 47-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-39 and 47-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10-18-1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 25-39 and 47, 48 and 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree (prior art-IDS, US Pat. 5783461) in view of Pedder (US Pat. 5717245) and Gilmour et al. (US Pat. 5391917).

A. Applicant's independent claims 25, 30, 35, 47, 52 and dependent claims 26-29, 31-34, 48-51 and 53 do not distinguish over Hembree, Pedder and Gilmour et al. regardless of the process for forming conductors comprising ablated portions, because only the final product is relevant, not the process of making such as "ablating using laser machining or drilling/etching". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process,

and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

B. Regarding claim 25, Hembree discloses a semiconductor component/package comprising:

- a composite substrate/interconnect (14/16 in Fig. 2) comprising a first surface with a conductive layer substantially covering the surface including traces/pads (58, 60, etc. in Fig. 2 and 4) and an opposing/second surface (31 in Fig. 2)
- a plurality of conductors/pairs of traces (58 in Fig. 4) comprising first contact members/pads (60 in Fig. 4) on a first end on the first surface (Fig. 4 and 5; Col. 6, line 21), each conductor comprising a plurality/pairs of conductor traces/pads having edges and spaces/grooves between the respective edges (edges/spaces/grooves not numerically referenced, see traces/conductors 58 in Fig. 4 and 5)
- the conductors/pairs of traces being defined using a metallization/etching (Col. 6, line 35) through the conductive layer having a thickness and configured for electrical connection with the semiconductor die, the conductors having a predetermined width/spacing (58/60- not numerically referenced in the plan view of Fig. 4) and being electrically isolated from one another by the spacings/grooves between the remaining portions of the conductive layer
- a semiconductor die on the first surface in electrical communication with the conductors (die 12 in Fig. 2)

- plurality of conductive lines/vias through the substrate/interconnect (49 in Fig. 3A) from the first contacts/first ends on the first surface to the second surface and in electrical communication with the conductors (40 in Fig. 2), and
- a plurality of external contacts/balls (38 in Fig. 2; Col. 4, line 53) in a ball grid array (BGA) on a second contacts/second ends of the conductors on the second surface in electrical communication with the conductive vias

(Fig. 2-5A; Col. 3, line 45- Col. 6, line 65).

Hembree shows the plan view (Fig. 4) of the conductors having edges, respective widths and spacings/grooves but fails to explicitly show a cross-section of the conductors having edges defined by the grooves.

Pedder teaches using a conductive layer (30 in Fig. 3, 80 in Fig. 9, etc.) substantially covering a first surface of substrate (12 in Fig. 3/9) and having conductive stubs/grooves/vias formed by a laser trimming through the conductive layer to the substrate (Col. 2, line 25, Col. 8, line 38; Fig.2, 3 and 9) in a multichip module/ball grid package. Pedder teaches forming such conductive pattern having edges defined by the stubs/grooves (not numerically referenced in Fig. 9, see edges/grooves between the conductors 94, 95, etc. in Fig. 9) using laser trimming/machining (Col. 8, line 45-54) which include a metallization/trace in first/X and second/Y directions. Pedder teaches using a conductor/trace wiring configuration where the wiring layout parameters such as spacing, pitch, number of conductor pads, vias, etc. are selected to achieve the desired electrical performance related to electrical signal, power/ground and impedance

requirements (Col. 5, line 11-Col. 6, line 50), the conductor pads having a pitch/spacing of 400 microns (Col. 5, line 15).

Gilmour et al. teach using a conductive layer (5 in Fig. 3-6; Col. 4, line 25-30; Col. 4 and 5) on a first surface of a substrate and forming a plurality of conductors/pads, lines having spacings/grooves using photo/etch processing and forming laser ablated/machined vias having a spacing of 40 microns (3/5 in Fig. 3; Col. 4, line 20-60) on the first surface of a substrate.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the plurality of conductors electrically isolated from one another by the grooves and separated by remaining portions of the conductive layer having edges defined by the grooves as taught by Pedder and Gilmour et al. so that the resonance characteristics and electrical performance of the interconnection can be improved in Hembree's component.

Regarding claim 26, Hembree teaches the semiconductor die being flip chip bonded/mounted or wire bonded to the plurality of bond pads on the conductors/substrate (56/60 in Fig. 4; Col. 6, line 21).

Regarding claim 27, Hembree teaches the semiconductor die being flip chip bonded/mounted to the plurality of bond pads on the conductors/substrate (56/60 in Fig. 4/5; Col. 6, line 21).

Regarding claim 28, Hembree teaches the substrate comprising a material selected from a group consisting of plastic, glass filled resin, silicon and ceramic (Col. 2, line 17-33; Col. 6, line 35).

Regarding claim 29, Hembree teaches the conductors comprising a plurality of contacts adapted for an external electrical connection to outside circuitry in a form of a ball/grid array (Fig. 2-3A; Col. 4, line 48).

Regarding claim 30, Hembree teaches substantially the entire claimed structure as applied to claims 25-27, including a method of forming the conductors using a conductive layer comprising a metal foil adhered/attached to the substrate (Col. 6, line 63-65; also see Col. 10, lines 20-23 as described in US Pat. 5634267 incorporated as a reference in Hembree).

Regarding claim 31, Hembree teaches substantially the entire claimed structure as applied to claims 25 and 30, including the conductors comprising a plurality of contacts adapted for an external electrical connection to outside circuitry (Fig. 2-3A; Col. 4, line 48).

Regarding claim 32, Hembree teaches substantially the entire claimed structure as applied to claims 25 and 30, including the plurality of conductive vias (49 in Fig. 3A) in the substrate in electrical communication with the conductors/traces and the plurality of external contact balls (38 in Fig. 2; Col. 4, line 53) on the second surface of the substrate.

Regarding claim 33, Hembree teaches substantially the entire claimed structure as applied to claims 25 and 30, including the semiconductor component comprising the package (Col. 1 and 2).

Regarding claim 34, Hembree teaches substantially the entire claimed structure as applied to claims 25 and 30, except an encapsulant at least partially covering the die and a portion of the surface.

Pedder teaches using a sealant/encapsulant to encapsulate the BGA package/module (Col. 1, line 55).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the encapsulant covering the die and a portion of the surface as taught by Pedder so that improved surface protection can be provided in Gilmour et al. and Hembree's semiconductor component.

Regarding claim 35, Hembree teaches substantially the entire claimed structure as applied to claim 25 above, including at least one pair of grooves in the conductive layer.

Regarding claim 36, Hembree teaches the semiconductor die being flip chip bonded/mounted or wire bonded to the plurality of bond pads on the conductors/substrate (56/60 in Fig. 4; Col. 6, line 21).

Regarding claim 37, Hembree teaches the conductors comprising a plurality of contacts/pads being adapted for an external electrical connection to outside circuitry in the form of a ball/grid array (Fig. 2-3A; Col. 4, line 48).

Regarding claim 38, Hembree teaches the substrate comprising a semiconductor material such as silicon and an insulating layer on the substrate (Col. 2, line 17-33; Col. 6, line 35).

Regarding claim 39, Hembree teaches the substrate comprising a material selected from a group consisting of plastic, glass filled resin, silicon and ceramic (Col. 2, line 17-33; Col. 6, line 35).

Regarding claim 47, Hembree teaches substantially the entire claimed structure as applied to claim 25, including the conductors comprising the first and second contacts on the first and second ends.

Regarding claim 48, Hembree teaches the semiconductor die being flip chip bonded/mounted or wire bonded to the plurality of bond pads on the conductors/substrate (56/60 in Fig. 4; Col. 6, line 21).

Regarding claim 51, Hembree teaches substantially the entire claimed structure as applied to claims 25 and 47 above, including the conductive layer/bonding area having an opening for attaching/wire bonding the die to the substrate (see 40/42 in Fig. 2; Col. 4, line 55; Col. 6, line 25).

Regarding claim 52, Hembree teaches substantially the entire claimed structure as applied to claim 25 above, including the plurality of vias (49 in Fig. 3A) through the substrate.

Regarding claim 53, Hembree teaches substantially the entire claimed structure as applied to claim 25, including the plurality of contact balls arranged in a BGA (38 in Fig. 2; Col. 4, line 53) on the substrate in electrical communication with the conductive vias.

3. Claims 49 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree (prior art-IDS, US Pat. 5783461), Pedder (US Pat. 5717245) and Gilmour et al. (US Pat. 5391917) as applied to claims 25 and 47 above, and further in view of Rostoker et al. (US Pat. 6181011).

Regarding claim 49, Hembree, Pedder and Gilmour et al. teach substantially the entire claimed structure as applied to claims 25 and 47 above, except each conductor having a first width of about 5 microns.

Rostoker et al. teach using a semiconductor component in a variety of packages including a BGA package where wiring/conductor dimensions such as width (W), spacing/groove size (S), thickness (T), etc. (Fig. 4) are optimized such that the width is in a range of 0.16-0.5 microns and a ratio W/S being in a range of 0.7-1.0 (Col. 10, lines 5- 30) in order to reduce the capacitance and interconnect delay and to improve the package performance (Col. 9, line 15- Col. 10, line 30).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate each conductor having a first width of about 5 microns as taught by Rostoker et al. so that the capacitance and interconnect delay can be reduced and the speed/performance of the package can be improved in Pedder, Gilmour et al. and Hembree's component.

Regarding claim 50, Hembree, Pedder and Gilmour et al. teach substantially the entire claimed structure as applied to claims 25 and 47 above, except each groove having a second width of about 5 microns.

Rostoker et al. teach using a semiconductor component in a variety of packages including a BGA package where wiring/conductor dimensions such as width (W), spacing/groove size (S), thickness (T), etc. (Fig. 4) are optimized such that the width is in a range of 0.16-0.5 microns and a ratio W/S being in a range of 0.7-1.0 (Col. 10, lines 5- 30) in order to reduce the capacitance and interconnect delay and to improve the package performance (Col. 9, line 15- Col. 10, line 30).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate each groove having a second width of about 5 microns as taught by Rostoker et al. so that the capacitance and interconnect delay can be reduced and the speed/performance of the package can be improved in Pedder, Gilmour et al. and Hembree's component.

Response to Arguments

4. Applicant's arguments filed on 10-11-02 have been fully considered but they are not persuasive.

A. Applicant contends that Hembree's conductors perform the same function but do not have grooves defined by the ablated portions of the conductive layer.

However, as explained above, only final product is relevant, not the process/method of forming conductor portions comprising spaces/grooves where the portions of the conductive layer can be laser ablated, chemically etched, plasma etched, or laser drilled/trimmed using the respective process technique.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh
05-16-03